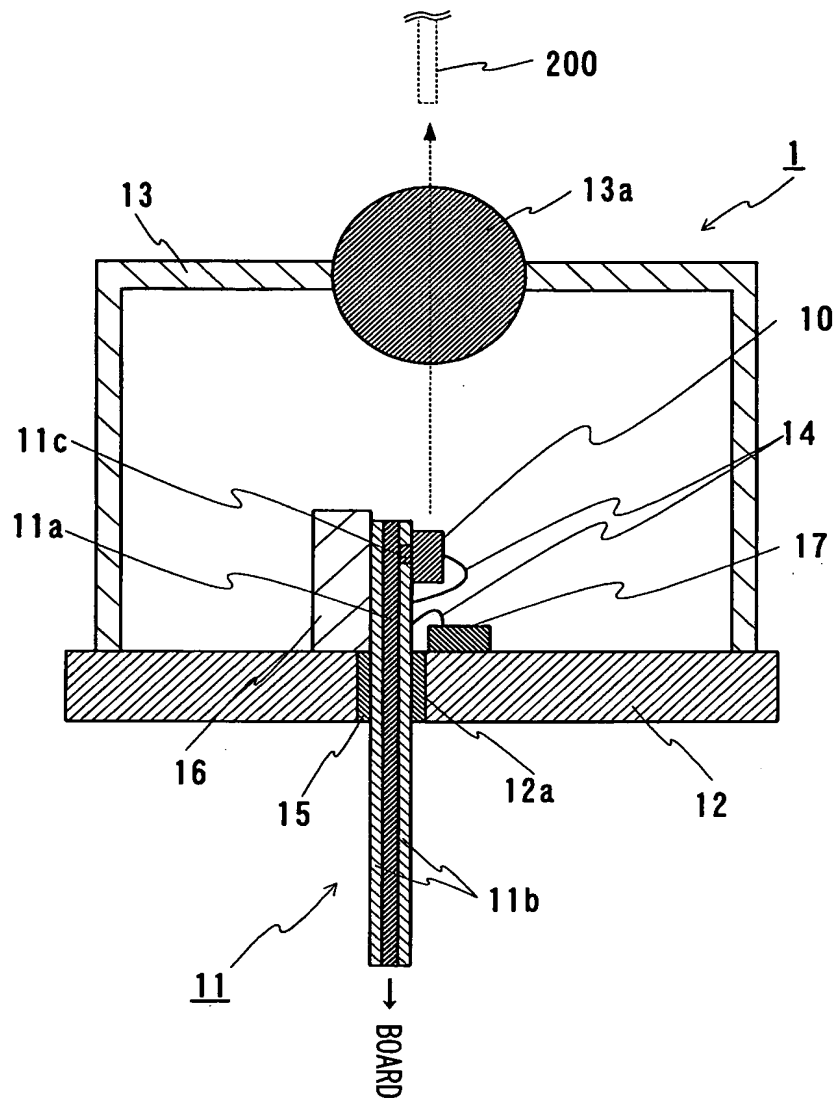


FIG. 1



[illegible]

A cross-sectional view of a semiconductor device 11A. The device features a substrate 11b with a patterned layer 11c. A gate stack 14 is formed on the substrate, with a gate electrode 20 and a gate insulating layer 21. A source/drain region 22 is formed in the substrate, with a contact plug 23. The device is labeled 11A at the bottom.

FIG. 3

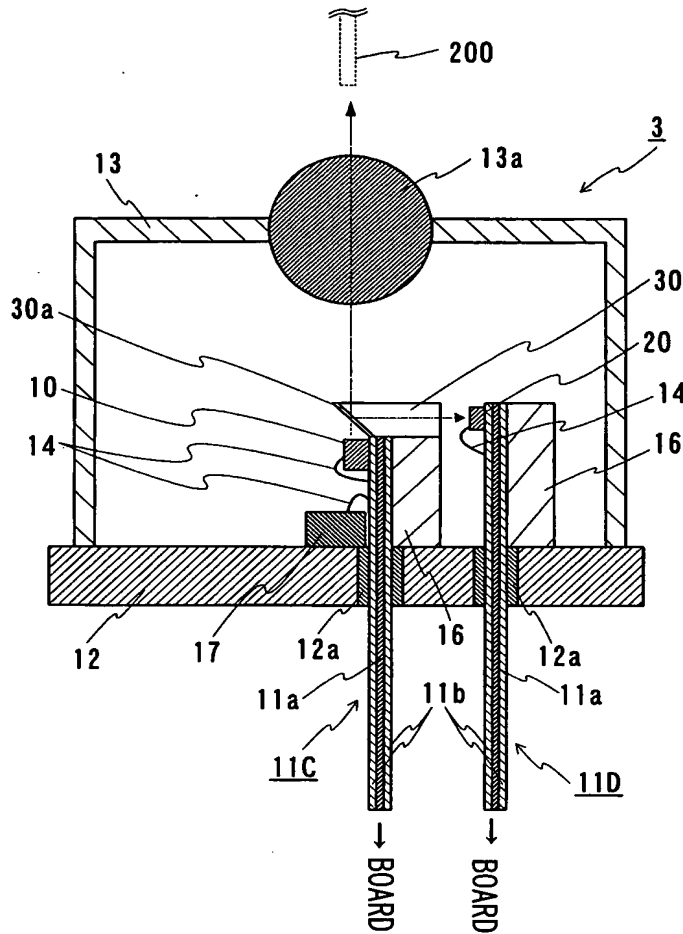


FIG. 4

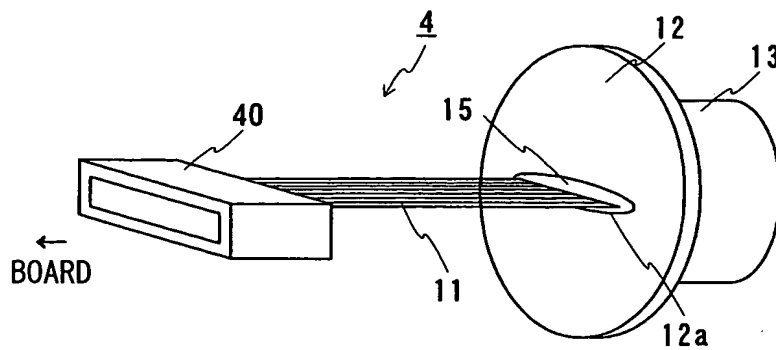


FIG. 5

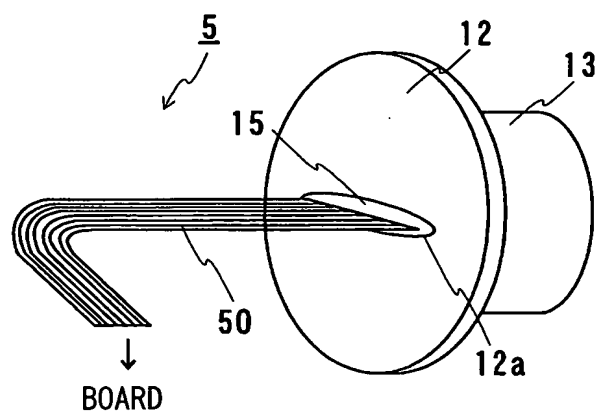


FIG. 6

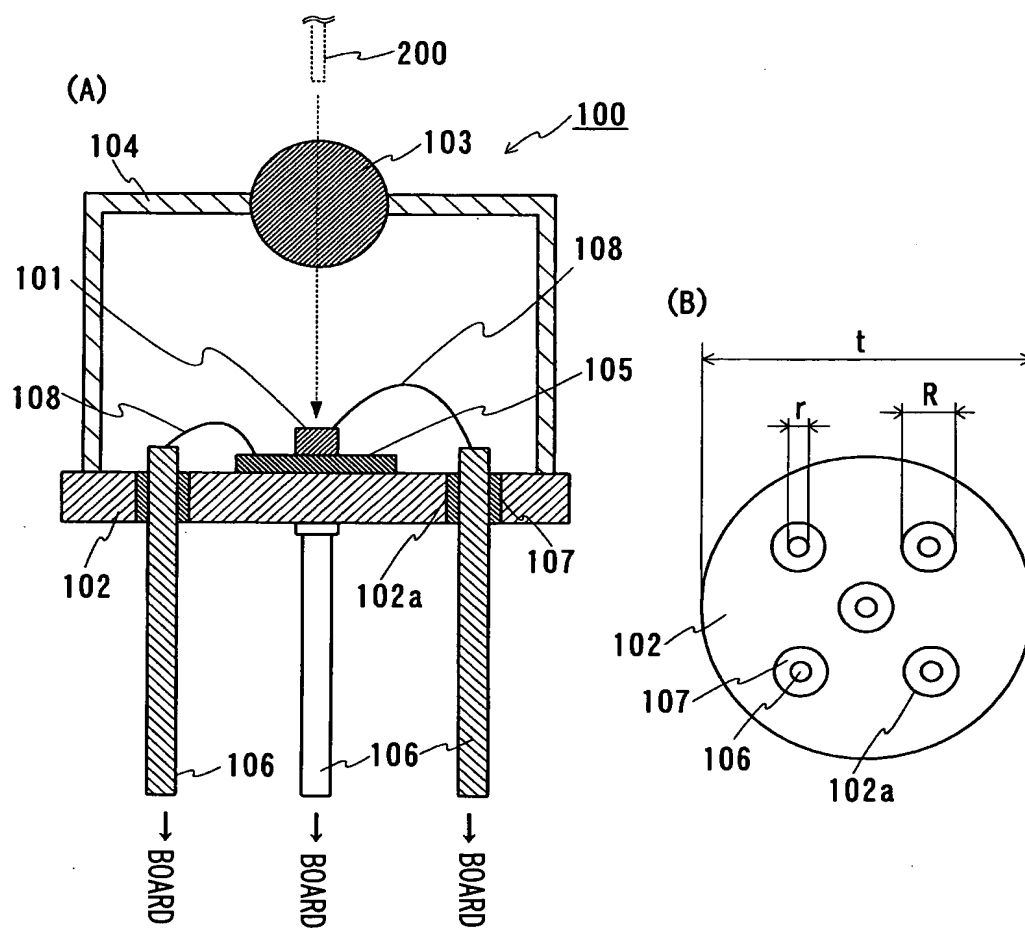


FIG. 7

